# Actions

## MICROELECTRONICS Co., Ltd.

## Actions-micro AM8352 Datasheet



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Revision History

| Version | Date | Description | Author |
|---|---|---|---|
| 1.0.0 | 11/09/2021 | Initial Create | maweishuo |

# Terms and Acronyms

| Terms and Acronyms | Definition |
|---|---|
| CF | Compact Flash |
| SM | Smart Media |
| XD | xD picture |
| SD | Secure Digital |
| Micro SD | Micro Secure Digital |
| MS | Memory Stick |
| MS Pro | Memory Stick Pro |
| MMC | Multimedia Card |
| SDRAM | Synchronous Dynamic Random Access Memory |
| MD | MicroDrive |
| TF | T Flash |
| LCD | Liquid Crystal Display |
| ICE | In-circuit emulation, or in-circuit emulator |
| JTAG | Joint Test Action Group(ANSI/ICEEE Std.11149.1-1990) |
| PQFP | Plastic Quad Flat Package |
| LQFP | Low-Profile Quad Flat Package |
| BGA | Ball Grid Array |
| PIP | Picture In Picture |
| TAP | TEST ACCESS PORT |
| RGB | Red-Green-Blue color space representation |
| TCON | Timing controller |
| | |
| | |

# General Conventions

| Symbol | Description | Notes |
|---|---|---|
| **Note** | | |
| H | In the notes column, an H indicates the pin is hidden behind the actual physical pin listed in the Alternate Functions column and is not included in the pin count. No H indicates the actual pin is listed in the Signal Name column and the Alternate Functions column lists the alternate signals present on the pin. | |
| **Pad GP** | | |
| 1 | Pad group 1 | |
| 2 | Pad group 2 | |
| **Dir/Pol (direction/polarity)** | | |
| I | Input | |
| O | Output | |
| B | Bidirectional | |
| Z | Three state output | |
| **Pad Type** | | |
| A | Analog pad | |
| B | Bidirectional | |
| BS | Bidirectional with Schmitt trigger | |
| H | High-voltage(up to 3.0 V)tolerant digital input | |
| I | CMOS input | |
| IA | Analog input | |
| IS | Input with Schmitt trigger | |
| K | Contains an internal weak keeper device | |
| O | Output | |
| OA | Analog output | |
| OD | Open-drain | |
| PD | Contains an internal pull-down device | |
| PP[NP] | Can be programmed to non pull, pull down or pull up. The default value is no pull after reset. | |
| PP[PD] | Can be programmed to non pull, pull down or pull up. The default value is pull down after reset. | |
| PP[PU] | Can be programmed to non pull, pull down or pull up. The default value is pull up after reset. | |
| PU | Contains an internal pull-up device | |
| PWR | power | |
| Z | High-Z output | |
| **Drive (mA)** | | |
| n | Variable drive strength pins. | |

# 1 Introduction

## 1.1 Overview

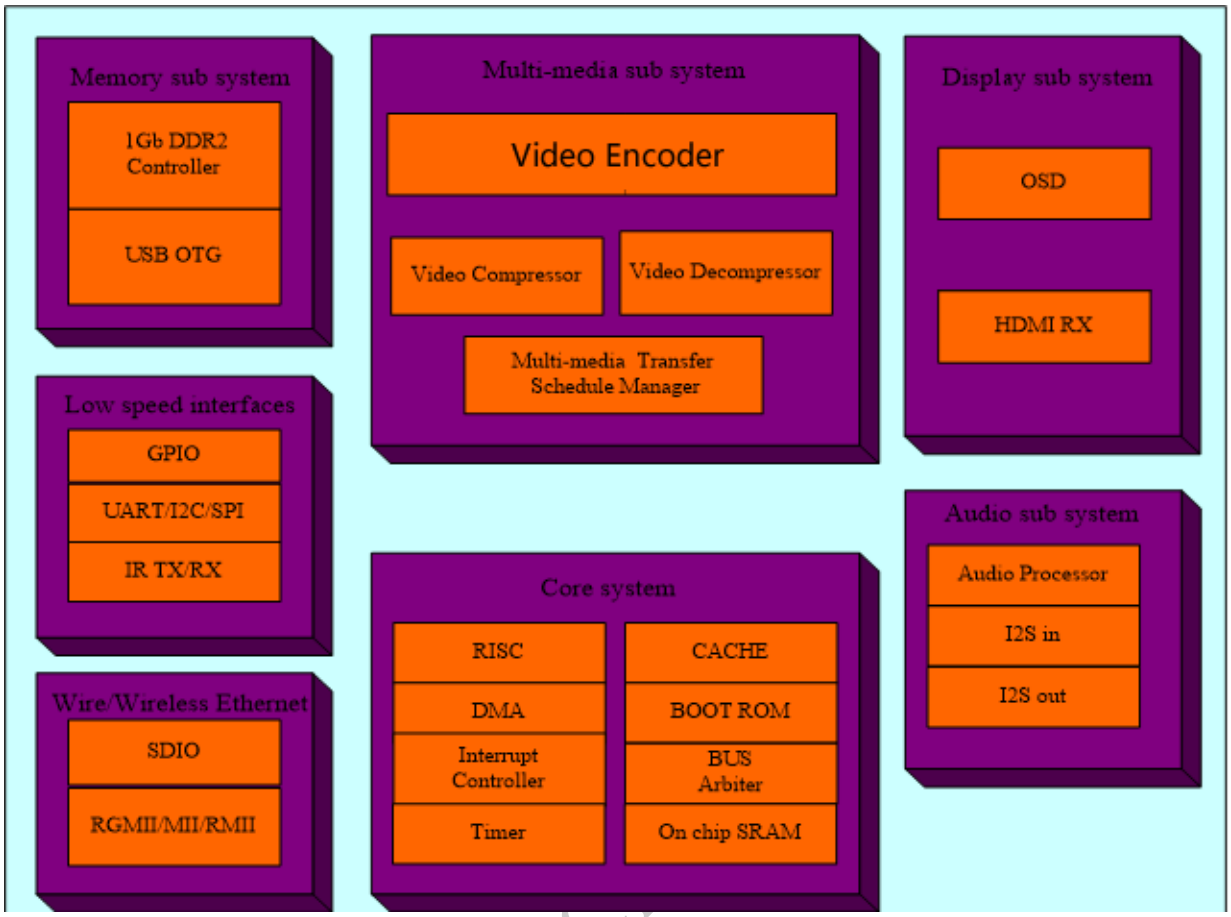
The AM8352 processor from Actions-Micro is a highly integrated mix signal SoC target at multi-media applications. The AM8352 emmedded CPU is a high performance, low power 32bit RISC core with DSP instruction extension, which can run as fast as 700MHz.

The AM8352 processor features a hardwired multi-format video encoder, which supports a large variety of popular video formats including: MJPEG/H.264 at full HD resolution.

The AM8352 multi-media processor provided display solutions with the help of on chip HDMI transmitter interface.

AM8352 is also integrated with 1 USB OTG controllers, UART, I2C, SPI, etc.

Block Diagram




AM8352 BLOCK DIAGRAM

# 2 Feature

The AM8352 provides high level of system integration to support a wide variety of applications. The features of the AM8352 include:

✓ **32BIT RISC CORE**
- 32K byte instruction cache and data cache
- F/W can program from DC up to 800MHz transparently
- DSP instruction for multi-media acceleration
- Static design allows changing clock at run-time for power saving

✓ **VIDEO ENCODER**
- Support ISO/IEC 14496-10/YU-T Rec.H.264
- Base Profile,Level 1-5.1
  - Main Profile ,levels 1-5.1
  - High Profile ,levels 1-5.1
- Support JPEG ITU-T Rec.T81(09/92),Baseline interleaved/JFIF
- 60 frames per second at 1920x1080 resolution for video all format

✓ **IMAGE/VIDEO COMPRESSOR**
- Support upto 1080P Resolution
- Support 8bit YCbCr 4:2:2 & YCbYCr/RGB
- Adaptive compress ratio up to 1:6

✓ **OSD**
- 1,2 OSD bitmap data width
- 256x128 size in 2 bit or 256x256 in 1 bit

✓ **DISPLAY INTERFACE**
- HDMI Rx support, industry standard compliance HDMI 1.3a

✓ **AUDIO**
- I2S IN & I2S OUT interface
- Support 32 levels volume control

✓ **MEMORY Storage**
- DDR2/3 SDRAM up to 4Gb @ 16bit up to 1066Mbps
- OTP ROM 64bit Chip ID

✓ **DMA CONTROLLER**
- 8 physical channels and 4 bus channels

- Stride mode support
- Software configurable priority

✓ **Boot ROM**
- On chip boot ROM with boot loader
- The system could be loaded from SPI Nor flash

✓ **USB 2.0 OTG**
- Complies with Universal Serial Bus Specification. Revision 2.0.
- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode.
- Supports full-speed or high-speed in peripheral mode.
- Supports USB Mass Storage Class Bulk-Only Transport Revision 1.0 as host or device.
- Supports Electronic still picture imaging Picture Transfer Protocol (PTP)
- Supports direct print function using pict-bridge
- Supports Universal Serial Bus Device Class Definition for Printing Devices Version 1.1 as host
- Supports Universal Serial Bus Still Image Capture Device Definition Revision 1.0 as host
- Configurable/programmable size of endpoints.
- Configurable/programmable single, double, triple or quad buffering.
- Programmable type of endpoints.
- Supports high-speed high-bandwidth Isochronous and Interrupt transfer.
- Supports suspend, resume and power managements function.
- Support USB wakeup

✓ **OTHER INTERFACE**
- UART/I2C/SPI
- 3 external interrupts
- 35 configurable GPIO shared with function pins

✓ **POWER**
- 1.3v for core
- 3.3v/2.5v/1.8/1.5v for mac io,3.3v for others
- Core PLL, LCD PLL,Audio PLL and DDR PLL support spread spectrum

✓ **PACKAGE**
- QFP 128pin (epad), 14x14mm

# 3 Power on Sequence

The power on sequence requirements of the AM7xxx and AM8xxx products are the same, which are shown in the following figure. VDD represents the power pins supplying power for the core. VCC represents the power pins supplying power for the general purpose pads. SVCC represents the power pins supplying power for the DDR2 or DDR3 SDRAM related pads. P_RESETB is the asynchronous reset pin. PWROK is an internal signal. It is low during the power-on phase to reset all the registers in the chip. The system boots at the moment when PWROK turns to high.

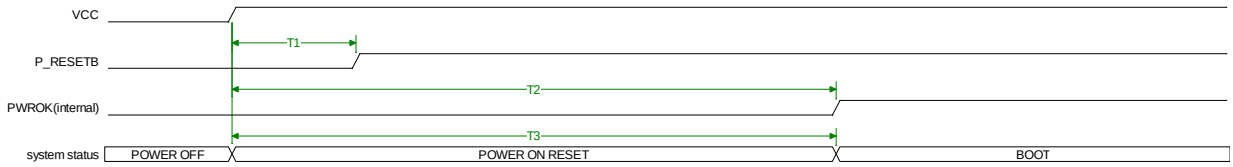



**Figure 1 Power on Sequence Diagram**

Timing Requirements:

1. $T1 \geq 20ms$
2. $T2 \approx 128ms$
3. $T3$ is equal to the greater one between $T1$ and $T2$
4. The power on sequence of VDD/VCC/SVCC is not cared

# 4 Pin Out Specification

Pin out table

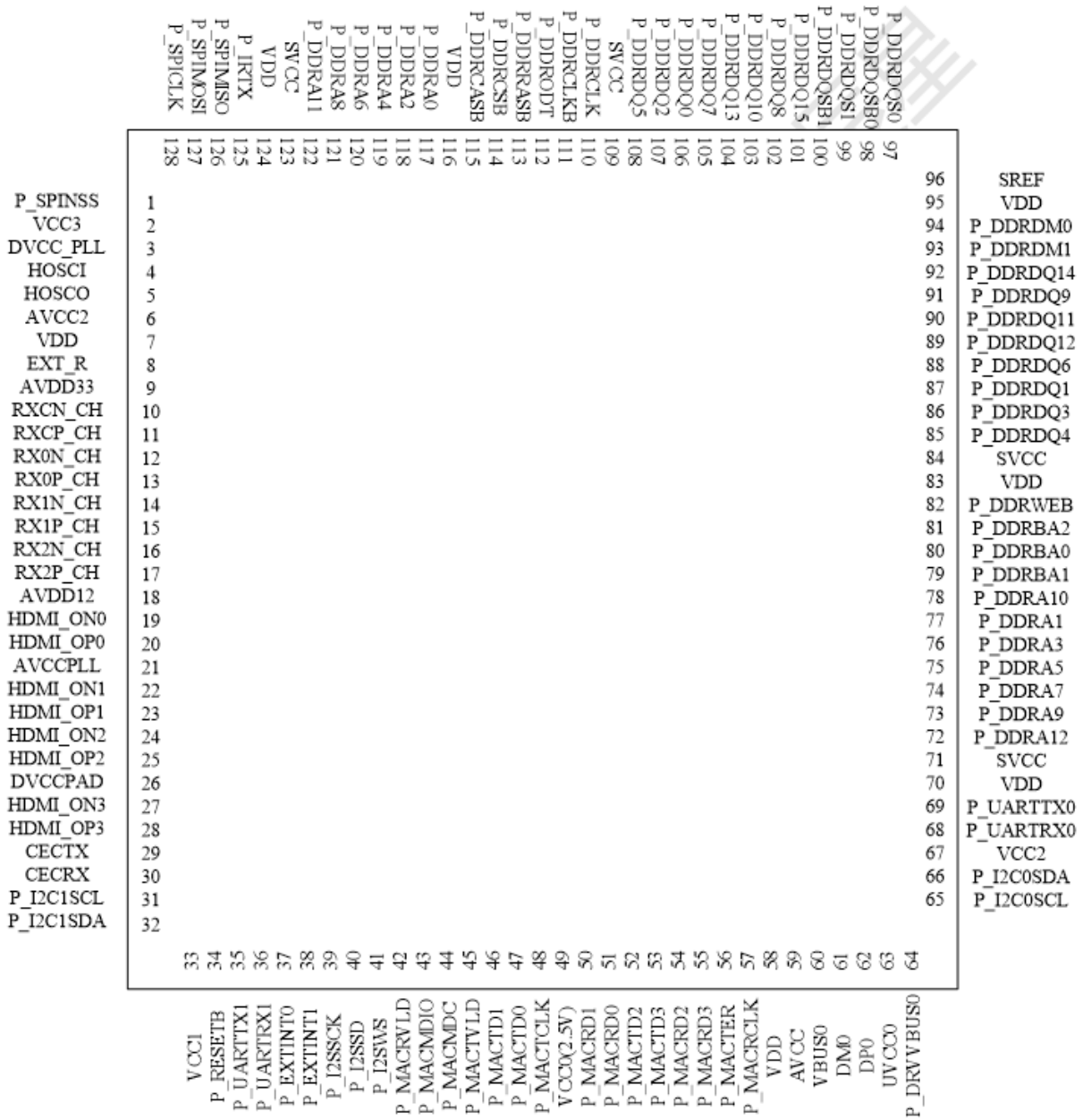
| PIN NUM | PIN NAME | TYPE | Function |
|---|---|---|---|
| 1 | P_SPINSS | B | SPI_NSS |
| 2 | VCC3 | PWR | VCC3 |
| 3 | DVCC_PLL | PWR | AVCC_PLL2 |
| 4 | HOSCI | A | HOSCI |
| 5 | HOSCO | A | HOSCO |
| 6 | AVCC2 | PWR | AVCC2 |
| 7 | VDD | PWR | VDD |
| 8 | EXT_R | A | EXT_R |
| 9 | AVDD33 | PWR | AVDD33 |
| 10 | RXCN_CH | A | RXCN_CH |
| 11 | RXCP_CH | A | RXCP_CH |
| 12 | RX0N_CH | A | RX0N_CH |
| 13 | RX0P_CH | A | RX0P_CH |
| 14 | RX1N_CH | A | RX1N_CH |
| 15 | RX1P_CH | A | RX1P_CH |
| 16 | RX2N_CH | A | RX2N_CH |
| 17 | RX2P_CH | A | RX2P_CH |
| 18 | AVDD12 | PWR | AVDD12 |
| 19 | HDMI_ON0 | A | HDMI_ON0 |
| 20 | HDMI_OP0 | A | HDMI_OP0 |
| 21 | AVCCPLL | PWR | AVCCPLL |
| 22 | HDMI_ON1 | A | HDMI_ON1 |
| 23 | HDMI_OP1 | A | HDMI_OP1 |
| 24 | HDMI_ON2 | A | HDMI_ON2 |
| 25 | HDMI_OP2 | A | HDMI_OP2 |
| 26 | DVCCPAD | PWR | DVCCPAD |
| 27 | HDMI_ON3 | A | HDMI_ON3 |
| 28 | HDMI_OP3 | A | HDMI_OP3 |
| 29 | CECTX | A | CEC_DAC |
| 30 | CECRX | A | CEC_DAC |
| 31 | P_I2C1SCL | B | I2C1SCL |
| 32 | P_I2C1SDA | B | I2C1SDA |
| 33 | VCC1 | PWR | VCC1 |
| 34 | P_RESETB | B | RESETB |
| 35 | P_UARTTX1 | B | GPIO17 |

| | | | |
|---|---|---|---|
| 36 | P_UARTRX1 | B | GPIO18 |
| 37 | P_EXTINT0 | B | EXTINT0 |
| 38 | P_EXTINT1 | B | GPIO32/I2STMCLK |
| 39 | P_I2SSCK | B | I2SSCK/IRRX |
| 40 | P_I2SSD | B | I2SSD/I2STSD |
| 41 | P_I2SWS | B | I2SWS/I2STWS |
| 42 | P_MACRVLD | B | RGMII_RXCTL |
| 43 | P_MACMDIO | B | MACMDIO |
| 44 | P_MACMDC | B | MACMDC |
| 45 | P_MACTVLD | B | RGMII_TXCTL |
| 46 | P_MACTD1 | B | RGMII_TXD0 |
| 47 | P_MACTD0 | B | RGMII_TXD1 |
| 48 | P_MACTCLK | B | RGMII_TXCLK |
| 49 | VCC0(2.5V) | PWR | VCC0(2.5V) |
| 50 | P_MACRD1 | B | RGMII_RXD1 |
| 51 | P_MACRD0 | B | RGMII_RXD0 |
| 52 | P_MACTD2 | B | RGMII_TXD2 |
| 53 | P_MACTD3 | B | RGMII_TXD3 |
| 54 | P_MACRD2 | B | RGMII_RXD2 |
| 55 | P_MACRD3 | B | RGMII_RXD3 |
| 56 | P_MACTER | B | MAC_CLKO |
| 57 | P_MACRCLK | B | RGMII_RXCLK |
| 58 | VDD | PWR | VDD |
| 59 | AVCC | PWR | AVCC |
| 60 | VBUS0 | A | VBUS0 |
| 61 | DM0 | A | DM0 |
| 62 | DP0 | A | DP0 |
| 63 | UVCC0 | PWR | UVCC0 |
| 64 | P_DRVVBUS0 | B | DRVVBUS0 |
| 65 | P_I2C0SCL | B | DDCSCL/GPIO20 |
| 66 | P_I2C0SDA | B | DDCSDA/GPIO21 |
| 67 | VCC2 | PWR | VCC2 |
| 68 | P_UARTRX0 | B | UARTRX0 |
| 69 | P_UARTTX0 | B | UARTTX0 |
| 70 | VDD | PWR | VDD |
| 71 | SVCC | PWR | SVCC |
| 72 | P_DDRA12 | B | P_DDRA12 |
| 73 | P_DDRA9 | B | P_DDRA9 |
| 74 | P_DDRA7 | B | P_DDRA7 |
| 75 | P_DDRA5 | B | P_DDRA5 |
| 76 | P_DDRA3 | B | P_DDRA3 |
| 77 | P_DDRA1 | B | P_DDRA1 |
| 78 | P_DDRA10 | B | P_DDRA10 |

| | | | |
|---|---|---|---|
| 79 | P_DDRBA1 | B | P_DDRBA1 |
| 80 | P_DDRBA0 | B | P_DDRBA0 |
| 81 | P_DDRBA2 | B | P_DDRBA2 |
| 82 | P_DDRWEB | B | P_DDRWEB |
| 83 | VDD | PWR | VDD |
| 84 | SVCC | PWR | SVCC |
| 85 | P_DDRDQ4 | B | P_DDRDQ4 |
| 86 | P_DDRDQ3 | B | P_DDRDQ3 |
| 87 | P_DDRDQ1 | B | P_DDRDQ1 |
| 88 | P_DDRDQ6 | B | P_DDRDQ6 |
| 89 | P_DDRDQ12 | B | P_DDRDQ12 |
| 90 | P_DDRDQ11 | B | P_DDRDQ11 |
| 91 | P_DDRDQ9 | B | P_DDRDQ9 |
| 92 | P_DDRDQ14 | B | P_DDRDQ14 |
| 93 | P_DDRDM1 | B | P_DDRDM1 |
| 94 | P_DDRDM0 | B | P_DDRDM0 |
| 95 | VDD | PWR | VDD |
| 96 | SREF | B | SREF |
| 97 | P_DDRDQS0 | B | P_DDRDQS0 |
| 98 | P_DDRDQSB0 | B | P_DDRDQSB0 |
| 99 | P_DDRDQS1 | B | P_DDRDQS1 |
| 100 | P_DDRDQSB1 | B | P_DDRDQSB1 |
| 101 | P_DDRDQ15 | B | P_DDRDQ15 |
| 102 | P_DDRDQ8 | B | P_DDRDQ8 |
| 103 | P_DDRDQ10 | B | P_DDRDQ10 |
| 104 | P_DDRDQ13 | B | P_DDRDQ13 |
| 105 | P_DDRDQ7 | B | P_DDRDQ7 |
| 106 | P_DDRDQ0 | B | P_DDRDQ0 |
| 107 | P_DDRDQ2 | B | P_DDRDQ2 |
| 108 | P_DDRDQ5 | B | P_DDRDQ5 |
| 109 | SVCC | PWR | SVCCI |
| 110 | P_DDRCLK | B | P_DDRCLK |
| 111 | P_DDRCLKB | B | P_DDRCLKB |
| 112 | P_DDRODT | B | P_DDRODT |
| 113 | P_DDRRASB | B | P_DDRRASB |
| 114 | P_DDRCSB | B | P_DDRCSB |
| 115 | P_DDRCASB | B | P_DDRCASB |
| 116 | VDD | PWR | VDD |
| 117 | P_DDRA0 | B | P_DDRA0 |
| 118 | P_DDRA2 | B | P_DDRA2 |
| 119 | P_DDRA4 | B | P_DDRA4 |
| 120 | P_DDRA6 | B | P_DDRA6 |
| 121 | P_DDRA8 | B | P_DDRA8 |

| | | | |
|---|---|---|---|
| 122 | P_DDRA11 | B | P_DDRA11 |
| 123 | SVCC | PWR | SVCC |
| 124 | VDD | PWR | VDD |
| 125 | P_IRTX | B | IRTX/I2STSCK |
| 126 | P_SPIMISO | B | SPI_MISO |
| 127 | P_SPIMOSI | B | SPI_MOSI |
| 128 | P_SPICLK | B | SPI_CLK |

## 4.1 Pin out diagram




AM8352 PIN-OUT DIAGRAM

# 5 Operating Conditions

Absolute Maximum Ratings

| SYMBOL | PARAMETER | RATING | UNITS |
|---|---|---|---|
| $V_{CC}$ | Power Supply (3.3V) | 3.8 | V |
| Vsvcc | Power Supply (1.5V) | 1.575 | V |
| $V_{dd}$ | Power Supply (1.35V) | 1.4 | V |
| $V_{IN}$ | Input Voltage | -0.5~4.6 | V |
| $V_{OUT}$ | Output Voltage | -0.5~4.6 | V |
| $T_{STG}$ | Storage Temperature | 0~75 | ℃ |
| Tc | Operation Temperature (Case Surface) | 0~70 | ℃ |
| Ta | Ambient Temperature | 0~60 | ℃ |

Recommended Operation Conditions

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply (3.3V) | 3.0 | 3.3 | 3.6 | V |
| Vsvcc | Power Supply (1.5V) | 1.425 | 1.5 | 1.575 | V |
| $V_{dd}$ | Power Supply (1.35V) | 1.3 | 1.35 | 1.4 | V |
| $T_a$ | Ambient Temperature | 0 | 35 | 60 | ℃ |

DC Electrical Characteristics for 3.3 volts operation

(Under Recommended Operating Conditions and $V_{CC}$ = 3.0V~3.6V, $T_j$ = 0 to +70 ) ℃

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | | | V |
| $V_{T-}$ | Schmitt Input Low Voltage | | | | 0.9 | V |
| $V_{T+}$ | Schmitt Input High Voltage | | 1.9 | | | V |
| $V_{OL}$ | Output Low Voltage | 4mA | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | 4mA | 2.4 | | | V |

# 6 Crystal Requirements

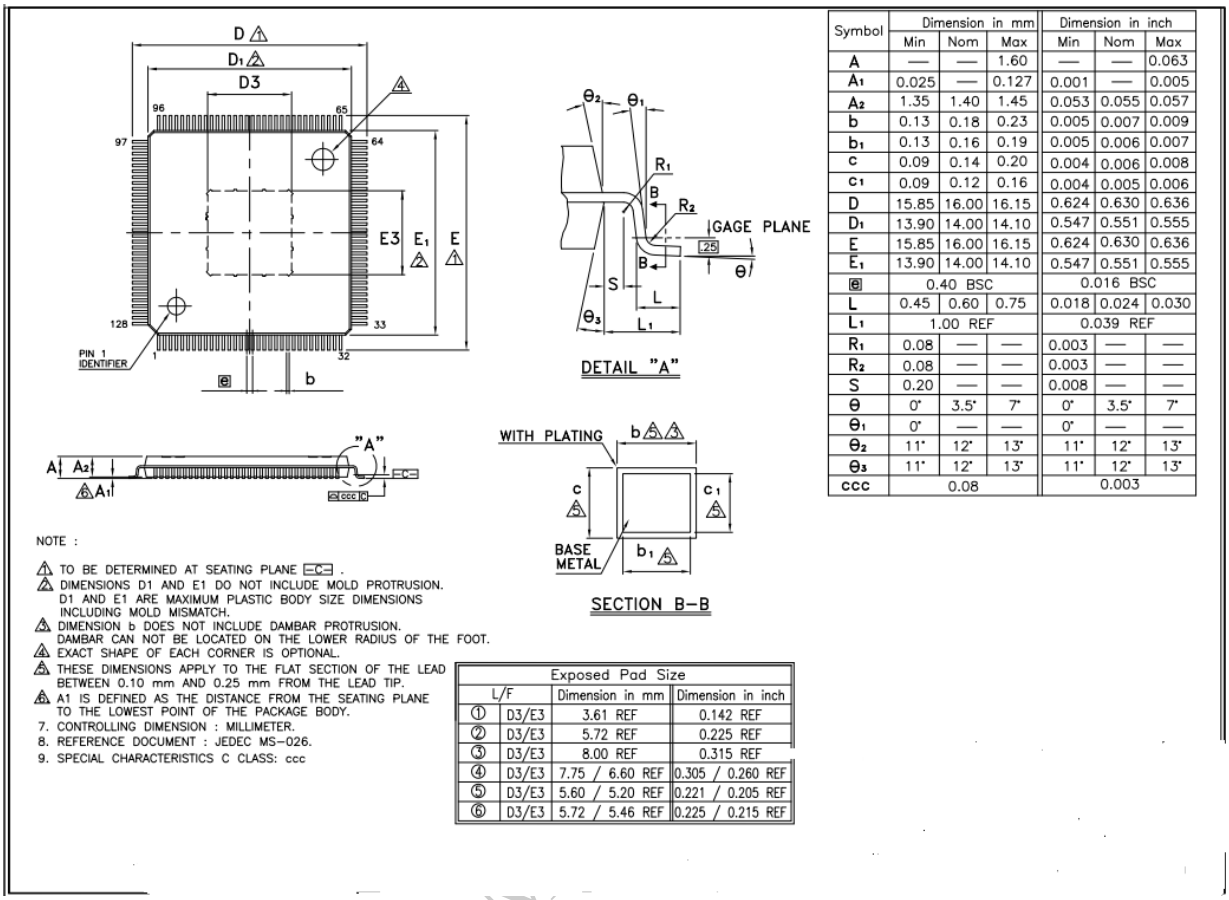
Requirements for 24MHz oscillator.

| Description | Specification Requirement |
|---|---|
| Nominal Frequency | 24MHz |
| Oscillation Mode | Fundamental |
| Frequency Tolerance at 25℃ | ±30ppm |
| Temperature Stability | ±50ppm |
| Shunt Capacitance (Co) | 7pF（max） |
| Load Capacitance (CL) | 12pF~18pF |
| Equivalent Series Resistance (ESR) | 50ohm（max） |
| Drive Level | 500uW （max） |
| Aging (at 25℃) | ±3ppm/year |
| Insulation Resistance | 10meg |
| Net Weight | This will be various. No limitation. |
| Operating Temperature Range | -10~85℃ |
| Storage Temperature Range | -45~125℃ |

Requirements for 32.768KHz oscillator.

| Description | Specification Requirement |
|---|---|
| Nominal Frequency | 32.768KHz |
| Oscillation Mode | Fundamental |
| Frequency Tolerance at 25℃ | ±30ppm |
| Temperature Stability | ±50ppm |
| Shunt Capacitance (Co) | 7pF（max） |
| Load Capacitance (CL) | 12pF~18pF |
| Equivalent Series Resistance (ESR) | 50ohm（max） |
| Drive Level | 500uW （max） |
| Aging (at 25℃) | ±3ppm/year |
| Insulation Resistance | 10meg |
| Net Weight | This will be various. No limitation. |
| Operating Temperature Range | -10~85℃ |
| Storage Temperature Range | -45~125℃ |

# 7 Mechanical Specification




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.025 | — | 0.127 | 0.001 | — | 0.005 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| b1 | 0.13 | 0.16 | 0.19 | 0.005 | 0.006 | 0.007 |
| c | 0.09 | 0.14 | 0.20 | 0.004 | 0.006 | 0.008 |
| c1 | 0.09 | 0.12 | 0.16 | 0.004 | 0.005 | 0.006 |
| D | 15.85 | 16.00 | 16.15 | 0.624 | 0.630 | 0.636 |
| D1 | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 15.85 | 16.00 | 16.15 | 0.624 | 0.630 | 0.636 |
| E1 | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| R1 | 0.08 | — | — | 0.003 | — | — |
| R2 | 0.08 | — | — | 0.003 | — | — |
| S | 0.20 | — | — | 0.008 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| ccc | 0.08 | | | 0.003 | | |

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

| Exposed Pad Size | | | |
|---|---|---|---|
| | L/F | Dimension in mm | Dimension in inch |
| ① | D3/E3 | 3.61 REF | 0.142 REF |
| ② | D3/E3 | 5.72 REF | 0.225 REF |
| ③ | D3/E3 | 8.00 REF | 0.315 REF |
| ④ | D3/E3 | 7.75 / 6.60 REF | 0.305 / 0.260 REF |
| ⑤ | D3/E3 | 5.60 / 5.20 REF | 0.221 / 0.205 REF |
| ⑥ | D3/E3 | 5.72 / 5.46 REF | 0.225 / 0.215 REF |